Echelon Product Brief

TouitInc. Application Specific Computing

Echelon

Echelon is a Real-Time Image Processor (RTIP) capable of performing 140,000 phase correlations per second. The images and templates for the phase correlation are stored in the on-board DDR2 SODIMM(s). The templates and the images are loaded into the DDR2 memory via the x1 PCI Express port. Images to be searched can also be loaded into the DDR2 memory through an external daughter module interface.

The daughter module interface allows Echelon to mate to a frame grabber. The available daughter module options are for a 4 channel ADS930 ADC, Camera Link, or a custom image acquisition interface. Echelon can also be ordered with an Ethernet interface to connect to GigE Vision enabled cameras.

Before being written into the DDR2 memory via the PCI Express port, the template images must first be processed. The preprocessing software is pointed to a directory on the disk drive containing the images to be converted for use as templates in the phase correlation board. It will convert each image to a 8 bit grayscale image, perform the 2D FFT, and then convert the result into compressed 16 bit complex number format.

This compression enables each 64x64 template image to be stored in 8KB of space on the DDR2 memory and thus enables quicker reading and loading of the template images into the phase correlation processor. Decompression is performed in the FPGA before being written into the memory of the phase correlation processor.

After the preprocessing, the templates can be loaded into various segments of the DDR2 memory. Beginning from byte address 0x0, to a register definable end address, can be configured for template image databases.

The remaining upper portion of the DDR2 memory is used as a 64x64 search image FIFO which can be written to from either the PCI Express bus or from the external daughter module interface. Once the FIFO has accumulated an entire 64 x 64 image, and with the proper CSR settings, the board can be configured to automatically perform phase correlations on incoming data and signal interrupts to the host computer when complete.

Each FIFO increment consists of 4128 bytes: 32 bytes for configuration and processing information and 4096 bytes for the 64x64, 8 bit grayscale search image. The configuration and processing information allows the user to set the start and end address locations in the DDR2 memory for the template database. If there are no settings enabled in the FIFO location being accessed, default values are loaded from the CSRs in the FPGA.

Being able to control the search range means multiple template image databases can be used on Echelon at the same time.

Even though Echelon deals in 64x64 byte increments, this does not mean the images have to be limited to that size. A 1024x1024 byte pixel image can be broken into 256 64x64 byte pixel segments. At 140,000 per second, Echelon can process roughly 546 1024x1024 images per second.

Echelon can be ordered with one or two DDR2 SODIMM. Echelon can be special ordered to process segment sizes other than 64x64. Obviously with the same FPGA, larger sized images will degrade the performance of the board.

Phase Correlation

Phase Correlation is the same as cross correlation, just computed differently. Instead of performing a convolution of two signals to obtain the cross correlation, with phase correlation the two signals are transformed into the frequency domain via an FFT and then multiplied together element wise. The magnitude is normalized and then the inverse FFT is applied.

The result is a peak (or peaks if there are multiple instances of the the template in the search signal) at the location where the two signals correlate. This peak indicates the translative offset between the two images.

One advantage of phase correlation over cross correlation is the result is less susceptible to certain types of noise, occlusions, and other defects typical of medical or satellite images. But the biggest advantage is the speed with which this computation can be performed versus the normal cross correlation.

Software Support

Touit provides both Windows and Linux support for Echelon. This includes the device drivers, API, a Python interface module, and sample programs.

The Python interface module allows users to interact with Echelon through the Python command interpreter. Providing Echelon users with a platform or environment that can support experimentation and algorithm trade-offs.

Python is the interface of choice because it is an open source interactive programming environment with a wide selection of open source libraries, particularly NumPy and SciPy for matrix and signal processing operations. Together these software tools provide an easy to use platform from which the application can quickly be tested and demonstrated. Which may ultimately become the final application.

Applications

Pattern & Image Recognition

Image Registration

Computer-aided Diagnosis Systems

Security Systems

Morphometrics